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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

INVENTORS: T.E. Fuehrer
K.E. Hollenbach
D.R. Laturell
S.B. Witmer

EXAMINER: R. SINGH

APPLICATION NO. 09/192,651

GROUP ART UNIT: 2644

FILED: November 16, 1998

TITLE: COMBINATION CLOCK AND CHARGE
PUMP FOR LINE POWERED DAA

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service on August 22, 2002, in an envelope as First Class Mail, postage prepaid, addressed to: Commissioner for Patents, Box AF, Attention: Board of Patent Appeals and Interferences, Washington, D.C. 20231.

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Lynn M. White
Lynn M. White

Commissioner for Patents
Box AF
Washington, D.C. 20231

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APPELLANTS' BRIEF

This brief is in furtherance of the Notice of Appeal filed in this case on April 23, 2002.

This brief is transmitted in triplicate.

1. **REQUIRED FEE**

A check in payment of the requisite fee (\$320.00) set forth in §1.17(f) and a two-month extension of time (\$400.00) is enclosed. The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Deposit Account No. 19-5425.

2. REAL PARTY IN INTEREST

The present application is assigned to **Agere Systems Guardian Corp.**, having its principal place of business at 555 Union Boulevard, Allentown, PA 18109. Accordingly, Agere Systems Guardian Corp. is the real party in interest.

3. RELATED APPEALS AND INTERFERENCES

The appellant, assignee, and the legal representatives of both are unaware of any other appeal or interference which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

4. STATUS OF CLAIMS

- A. Claims canceled: None
- B. Claims withdrawn from consideration but not canceled: None
- C. Claims pending: 1-19
- D. Claims allowed: None
- E. Claims rejected: 1-19
- F. Claims appealed: 1-19

Appealed claims 1-19 as currently pending are attached as Appendix A hereto.

5. STATUS OF AMENDMENTS

An amendment after final (37 C.F.R. 1.116) was filed in the present case on February 25, 2002, and amendments to claims 15 and 18 were submitted therein. The Examiner entered these amendments for the purpose of this appeal. Claims 1, 2, 7, 8, and

9 were amended in a Reply and Amendment under 37 C.F.R. §§1.111 and 1.115 filed on August 10, 2001 and resulted in the final Office Action appealed herein. In the same Reply and Amendment, claims 14 - 19 were added.

6. SUMMARY OF THE CLAIMED INVENTION

The present invention relates to an interface utilizing existing clock signals from a driver circuit, such as a DSP, to charge capacitors that are normally used for capacitive coupling of digital data across a high voltage isolation barrier. Using relatively small capacitors (e.g., capacitors in the range between 10 pF and 500 pF, and preferably at 100 pF) a charge pump is formed to generate power to the interface at all times. Thus, the interface always has a steady source of power available for use, including during the on-hook state, for powering circuitry that can detect, modulate, and transmit on-hook signals across the capacitive interface.

The claimed invention includes circuitry that doubles the voltage of the clock signal coming from the DSP, thereby obtaining more power for use by a data access arrangement (DAA) coupled to the interface and, therefore to the DSP. Further, the interface circuit is a fully differential circuit, thereby eliminating the need to keep the impedance across the capacitive coupling low, as is required when using a pseudo-differential interface circuit.

7. ISSUES

A. 35 U.S.C. §112 ISSUES INVOLVING CLAIMS 1-19

1. Whether the Examiner improperly rejected the claims under 35 USC § 112, first paragraph, because of the “doubling limitation” (claim 1) and the “capacitance sufficient to create a charge pump limitation”;

B. ISSUES INVOLVING CLAIMS 1-13, 15, 16, 18 AND 19

1. Whether the Examiner improperly rejected the claims because the cited prior art fails to teach or suggest an interface that includes a circuit, a charge pump that doubles the voltage of a clock signal provided by a driver circuit to thus increase the voltage available for use by a data access arrangement (DAA).

C. ISSUES INVOLVING CLAIMS 14 AND 17

1. Whether the Examiner properly rejected the claims because the cited prior art fails to teach or suggest a fully differential interface circuit that includes a DSP generating a clock signal having a voltage, a DAA, and a charge pump coupled between the DSP and DAA to provide operating power to the DAA and to double the voltage of the clock signal.

8. GROUPING OF CLAIMS

- A. Claims 1-6, 8-13, 15, 16, 18 and 19 stand or fall together.
- B. Claim 7 stands or falls on its own.
- C. Claims 14 and 17 stand or fall together

9. ARGUMENT

A. The Specification Supports the Doubling of the Voltage of the Clock Signal by the Charge Pump

Claims 1 and 8 recite the following limitation: "said charge pump doubling the voltage of said clock signal." Claim 7 recites the following limitation: "generating a power signal, having a voltage, across said charge pump by inputting the output of said clock generator to said charge pump; and doubling the voltage of said power signal and storing said generated power signal for use by said interface," The Examiner asserts that these limitations are not supported by the specification. Applicant respectfully disagrees, and refers the Board to the specification, page 7, lines 6-7: "Diodes D1, D2 and D3 rectify and double the clock signals for the purpose of charge pumping." Further, it would be abundantly evident to one of ordinary skill in the art that the diode configuration of D1, D2, and D3 in Figure 2 will double the voltage of the clock signal. Thus, the specification clearly supports this limitation.

B. The Specification Supports the Recitation in Claims 15 and 18 of a Capacitive Element of a Capacitance Sufficient to Create the Charge Pump of the Present Invention

In response to a rejection of claims 15 and 18 based on the limitation, "a maximum capacitance of 500 pF; and a minimum capacitance of 10 pF", Applicant amended claims 15 and 18 to recite the limitation "a capacitance sufficient to create said charge pump" and asserted that this limitation was clearly supported by the specification. The Examiner has entered this amendment, and has not provided any 35 USC 112 grounds for rejecting these claims. Thus, the Examiner has accepted this amendment as overcoming the 112 rejection originally asserted in the Final Office Action. By way of information, however, applicant

points to page 7, lines 14-25, of the specification, where support for this limitation is found.

C. The Claims Are Patentable Over the Prior Art

1. Hein et al., U.S. Patent No. US 6,198,816 B1

U.S. Patent No. 6,198,816 to Hein et al. ("Hein") teaches a communication system utilizing a capacitive isolation barrier to linearly attenuate the tip/ring signal voltage levels from the high phone line levels to levels within integrated circuit technology limitations. The Hein isolation circuit illustrated, for example, in Fig. 13A and Fig. 13B, is a pseudo-differential circuit, because receiver 262 of Fig. 13b is not a differential receiver. At best, Hein illustrates a pseudo-differential circuit.

The capacitive isolation barrier of Hein requires very large capacitors, e.g., at least 10,000 pF. With the large capacitances required by Hein, the impedance is low with respect to the signals across the capacitance; thus, Hein must use extensive filtering to filter out existing common mode signals and also common mode signals generated by the interface itself if lower capacitances were used in connection with the pseudo-differential circuit.

2. Hershbarger et al., U.S. Patent No. 5,664,984

U.S. Patent No. 5,664,984 to Hershbarger et al. ("Hershbarger") teaches a method and apparatus for communicating a modulated signal across an isolation barrier using capacitors, similar to the capacitive isolation barrier of Hein. Like Hein, Hershbarger utilizes a pseudo-differential circuit which is thus very sensitive to impedance, thereby

requiring that the capacitive coupling have a high value, e.g., 10,000 pF. Hershberger is relied upon by the Examiner for its teaching of the use of a DSP with a charge pump for high voltage isolation for a DAA.

3. Kan et al., U.S. Patent No. 6,020,773

U.S. Patent No. 6,020,773 to Kan et al. ("Kan") teaches a clock signal generator for generating a plurality of clock signals with different phases.

The Examiner has not Established a *prima facie* Case of Obviousness

As set forth in the MPEP:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143

The Examiner has not met the above criteria.

As noted above, to support a rejection under 35 U.S.C. §103, the cited references must suggest a reason, suggestion, or motivation to lead an inventor to combine two or more references. With respect to claims 1-6, 8-13, 15, 16, 18, and 19, none of the references cited by the Examiner teach or suggest a charge pump that doubles the voltage of a clock signal provided by the driver circuit to thus increase the voltage available for use by a DAA. With respect to Claim 7, none of the cited references teach or suggest generating a power voltage across a charge pump and then doubling that voltage for use by the interface. In addition, none of Hein, Hershberger, or Kan teach or suggest the use of a

fully differential signal processing circuit, and thus each requires very large value capacitors, and/or filtering elements if the size of the capacitors are reduced.

These novel and distinguishing features are included in each of claims 1-13, 15, 16, 18, and 19 (claim 1, "a charge pump ... doubling the voltage of said clock signal"; claim 7, "a charge pump between said DSP and said DAA ...; doubling the voltage of said power signal ..."; claim 8, "a charge pump ... doubling the voltage of said charge and passing said doubled voltage to said DAA to provide said operating power."; claim 15, "An interface circuit as set forth in claim 2 wherein said first capacitive element has a capacitance sufficient to create said charge pump."). Since none of these elements are taught or suggested by Hein, Hershbarger or Kan, it is submitted that claims 1-13, 15, 16, 18 and 19 patentably define over the cited references.

Regarding claims 14 and 17, none of Hein, Hershbarger or Kan teach or suggest the use of a fully differential signal processing circuit, and thus each of the developments disclosed in these references require very large capacitors, and/or filtering elements if the size of the capacitors are reduced. These novel and distinguishing features are included in each of claims 14 and 17 (claim 14, "An interface circuit as set forth in claim 1, wherein said interface circuit is a fully differential circuit"; claim 17, "An interface circuit as set forth in claim 8, wherein said interface circuit is a fully differential circuit."). Since none of these elements are taught or suggested by Hein, Hershbarger or Kan, it is submitted that claims 14 and 17 patentably define over the cited references.

Discussion of Examiner's Comment in the Advisory Action

Applicants maintain their assertion that the claimed invention is a fully differential circuit and that the Hein circuit is a pseudo-differential circuit.

The present invention uses a differential charge pump and differential transmission circuit because of undesirable common mode voltages that may be present. The present invention rejects common mode voltages of any level, regardless of the value of the capacitors because of the differential charge pump and differential transmission circuit. By contrast, the circuit of Hein will fail in the presence of a large common mode voltage. This is readily apparent to one of ordinary skill in the art. As an example, a typical 150 volt peak-to-peak common mode voltage presented across the Hein circuit will cause it to fail, while the same 150 volt peak-to-peak voltage across the present invention will not inhibit the present invention in any way.

In the Advisory Action, the Examiner stated the following.

"Hein et al (U.S. Patent No. 6,198,816) teaches a preferred embodiment for a clock recovery circuit 216 for use in this invention detailed in in Figure 5 and described [as follows]. One section of the clock recovery circuit may be a phase locked loop ("PLL") circuit, consisting of phase/frequency detector 532, charge pump 532, resistor 533, capacitor 534, and voltage controlled oscillator ("VCO") 535. The other section of the clock recovery block is data latch 542 operating outside the phase locked loop to re-time the digital data received across the isolation barrier. Circuitry for performing these functions is well known to those skilled in the art. See, for example, F. Gardener, *Phaselock Techniques*, 2d ed., John Wiley & Sons, NY, 1979; and R. Best, *Phase-Locked Loops*, McGraw Hill, 1984, which are incorporated herein by reference. The data input to the receive system from the isolation capacitors may be derived from a differential signal present at the barrier by passing the differential signal through MOS input buffers (not shown), which are well known in the art, and providing a single-ended binary output signal 530 to the clock recovery circuit (col. 12, lines 59-67; col. 13, lines 1-10). Clearly, Hein et al. discloses a combination of a clock and charge pump for line-powered DAA."

The Examiner's statements in the Advisory Action are improper for several reasons. First, the Examiner cites, and in fact incorporates by reference, the entire text of "Phaselock Techniques", 2d ed. By F. Gardener (182 pages) and "Phase-Locked Loops", by R. Best (373 pages) for an alleged teaching of a clock recovery block comprising a data latch.

Nowhere does the Examiner identify where within the 555 pages of text this alleged teaching apparently exists. Perhaps more important, however, is that the above statement, like all of the other statements made by the Examiner in this prosecution, fails to show that any of the cited references teach or suggest (A) a charge pump doubling the voltage of a DSP and providing operating power to a DAA or (B) a fully differential circuit having a charge pump doubling the voltage of a DSP and providing operating power to a DAA. The art does not teach or suggest it, the Examiner does not and cannot point to any place in the art where it does, and thus the rejections made are improper.

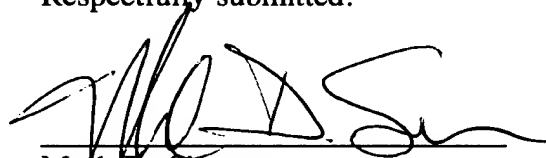
Applicants submit that the claims meet the requirements of 35 U.S.C. §112 and that no *prima facie* showing of obviousness has been made and respectfully requests that the Board reverse the Examiner's rejection and allow the claims.

10. CONCLUSION

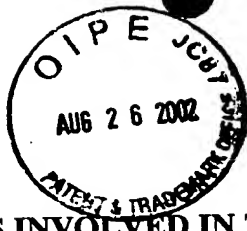
For the foregoing reasons applicants respectfully request this Board to overrule the Examiner's rejections and allow claims 1-19.

Respectfully submitted:

August 22, 2002
Date


Mark D. Simpson
Registration No. 32,942

Synnestvedt & Lechner LLP
2600 Aramark Tower
1101 Market Street
Philadelphia, PA 19107
Telephone: 215-923-4466
Facsimile: 215-923-2189



APPENDIX A

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CLAIMS INVOLVED IN THIS APPEAL:

1. An interface circuit, comprising:
a digital signal processor (DSP) generating a clock signal having a voltage;
a data access arrangement (DAA); and
a charge pump, coupled between said DSP and said DAA, said charge pump providing operating power to said DAA, said charge pump doubling the voltage of said clock signal.
2. An interface circuit as set forth in claim 1, wherein said charge pump comprises:
a first capacitive element having an input side connected to said DSP and an output side connected to said DAA;
a second capacitive element having an input and an output each connected to said DAA; and
a rectifying element coupled between the output side of said first capacitive element and said second capacitive element, said rectifying element receiving said clock signal from said DSP and doubling the voltage of said clock signal before passing said clock signal to said DAA.
3. An interface circuit as set forth in claim 2, wherein said DSP includes a clock generator generating first and second clock pulses out of phase with each other by 180° and wherein said first capacitive element comprises:
a first capacitor coupled to receive said first clock pulse; and
a second capacitor coupled to receive said second clock pulse, wherein said first capacitive element continuously outputs a positive output voltage to said rectifying element.
4. An interface circuit as set forth in claim 3, wherein said rectifying element comprises a diode rectifier.
5. An interface circuit as set forth in claim 4, wherein said DAA includes a clock regeneration element connected in parallel with said rectifying circuit to remove DC level shift and regenerate a clock pulse for use by the DAA which is essentially identical to the clock pulse output by said clock generator.

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6. An interface circuit as set forth in claim 5, wherein said second capacitive element comprises a storage capacitor which stores the charge transferred by said first and said second capacitors.

7. A method of providing power to a data access arrangement (DAA) in an interface circuit of a telecommunication network when a telephone line connected to said interface circuit is in the on-hook state, said interface circuit including a digital signal processor (DSP) having a clock generator, said method comprising the steps of:

- inserting a charge pump between said DSP and said DAA;
- generating a power signal, having a voltage, across said charge pump by inputting the output of said clock generator to said charge pump; and
- doubling the voltage of said power signal and storing said generated power signal for use by said interface.

8. An interface circuit, comprising:

- a driver circuit for developing a charge across capacitive elements of said interface circuit, said charge having a voltage;
- a data access arrangement (DAA); and
- a charge pump, coupled between said DAA and said driver circuit, said charge pump providing operating power to said DAA, said charge pump doubling the voltage of said charge and passing said doubled voltage to said DAA to provide said operating power.

9. An interface circuit as set forth in claim 8, wherein said charge pump comprises:

- a first capacitive element having an input side connected to said driver circuit and an output side connected to said DAA;

- a second capacitive element having an input and an output each connected to said DAA; and

- a rectifying element coupled between the output side of said first capacitive element and said second capacitive element, said rectifying element receiving said charge from said driver circuit and doubling the voltage of said charge before passing said charge to said DAA.

10. An interface circuit as set forth in claim 9, wherein said driver circuit comprises a clock generator generating first and second clock pulses out of phase with each other by 180° and wherein said first capacitive element comprises:

a first capacitor coupled to receive said first clock pulse; and
a second capacitor coupled to receive said second clock pulse, wherein said first capacitive element continuously outputs a positive output voltage to said rectifying element.

11. An interface circuit as set forth in claim 10, wherein said rectifying element comprises a diode rectifier.

12. An interface circuit as set forth in claim 11, wherein said DAA includes a clock regeneration element connected in parallel with said rectifying circuit to remove DC level shift and regenerate a clock pulse for use by the DAA which is essentially identical to the clock pulse output by said clock generator.

13. An interface circuit as set forth in claim 12, wherein said second capacitive element comprises a storage capacitor which stores the charge transferred by said first and said second capacitors.

14. An interface circuit as set forth in claim 1, wherein said interface circuit is a fully differential circuit.

15. An interface circuit as set forth in claim 2, wherein said first capacitive element has a capacitance sufficient to create said charge pump.

16. An interface circuit as set forth in claim 2, wherein the first capacitive element has a capacitance value of approximately 100 pF.

17. An interface circuit as set forth in claim 8, wherein said interface circuit is a fully differential circuit.

18. An interface circuit as set forth in claim 9, wherein said first capacitive element has a capacitance sufficient to create said charge pump.

19. An interface circuit as set forth in claim 9, wherein the first capacitive element has a capacitance value of approximately 100 pF.